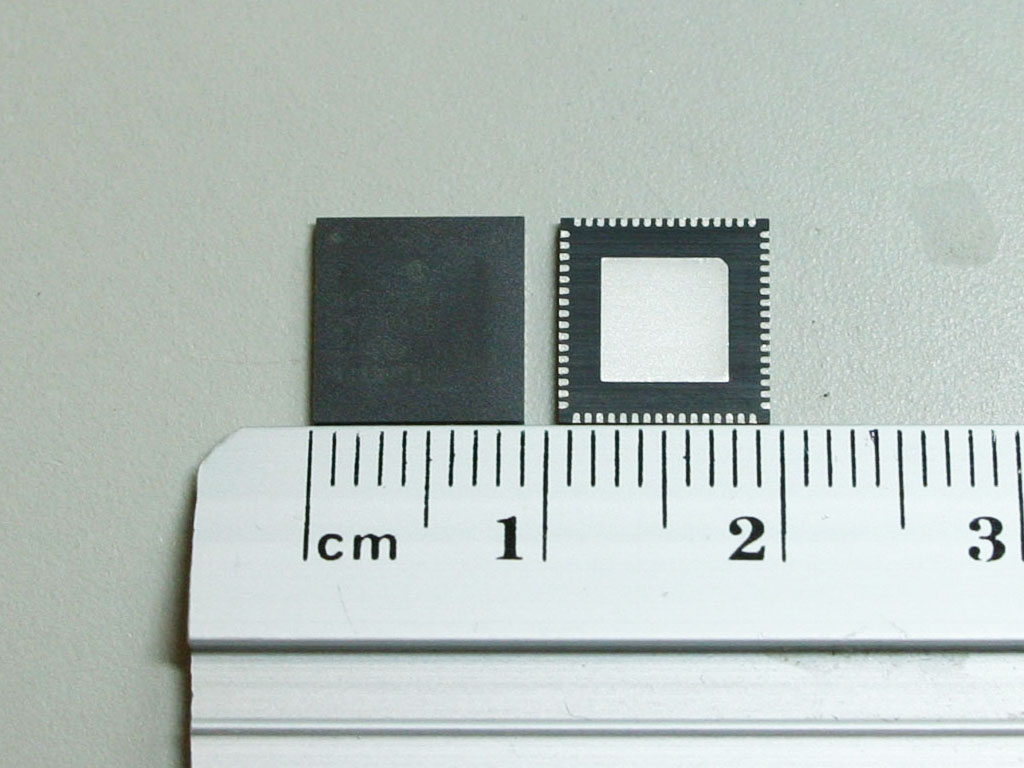
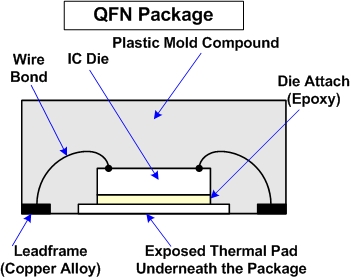
# QFN – Quad Flat No-lead(方形扁平无引脚封装)





## Thermal implications

Flat no-lead packages include an exposed thermal pad to improve heat transfer out of the IC (into the PCB). Heat transfer can be further facilitated by metal vias in the thermal pad.

The exposed copper die-pad technology offers good thermal and electrical performance.

It also provides excellent thermal performance through exposed leadframe pads with a direct thermal path to dissipate heat from the package. The thermal pad is typically soldered directly to the board, and the thermal vias in the PCB help to dissipate excess power into the copper ground plane to absorb excess heat.

## Effects of vibrations

QFN stress issue should be caused by vibration effect due to leads resonance & mechanical bouncing. Normally worst affected area was at peripheral, but center units could also fail.

Certain clamping condition could cause significant amount of vibrations that affected stability of neighbor leads. The poor stability condition was believed to be one of the major impacting factors that worsen the resonance effect, generating more risks to wire stress issues. The better clamping condition was developed by optimization of clamping hardware design, and clamping force. The optimum clamping condition could reduce the mechanical vibration and hence keeping minimum impact to leads of neighbor units, especially during resonance effect.

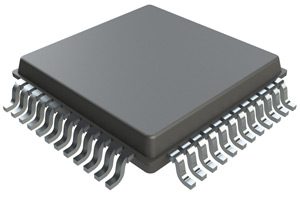
## Package size vs I/Os

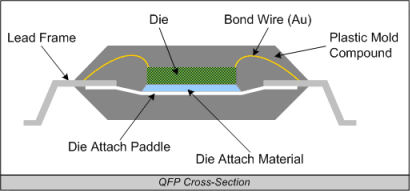
Eliminated the external lead laterally protruding out of the package that consume lots of space. So this can make QFN as thin as possible. Because there is no extension lead, so it is hard to damage.

The number of I/Os approaches that of CSP/FBGA packages with the advantages of lower cost for portable and telecommunication applications.

QFN package have advantages in package size and thermal implications.

# QFP – Quad Flat Pack(方型扁平式封装)

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## Thermal implications

QFP uses a buried metal sheet to improve heat dissipation and mostly used in high frequency circuits, but i think the thermal performance is not good at QFN because of the heat dissipation area.

A more challenging thermal issue is the thermal cyclic stress in a QFP component may experience during its operational life. When chips are running hotter, it increases the difference in temperature between itself and the leads as well as solder material. Leads or solder joint fracture or fatigue failure always occur even through multiple electronic package designs kept trying to fix it . As package size shrinks, the heat generated in die is increasing the mismatch in the coefficients of thermal expansion (CTE) between the leads and solder material since the distance is closer between chip and leads which reduced the heat transfer process. The optimization for the package design with fine pitch leads is expected.

## Effects of vibrations

Due to the random vibration load conditions, the QFP device solder joints are subjected to alternating stress, resulting in solder joint failure.

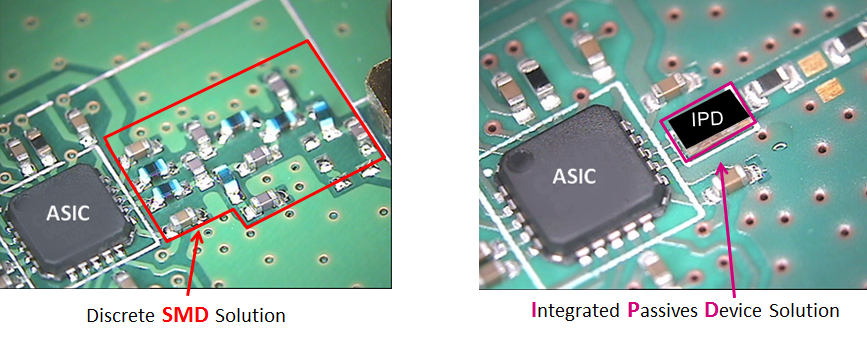
## Package size vs I/Os

The ratio between chip area and package area is small.

The technology realizes that the distance between the pins of the CPU chip is small, the pins are very thin, and the large-scale or very large-scale integrated circuits generally adopt this package form, and the number of pins thereof is generally above 100.

QFP package have advantages in package size vs I/Os.

# IPD – Integrated Passive Device(集成无源元件)

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## Thermal implications

IPDs are generally fabricated using standard wafer fabrication technologies such as thin film and photolithography processing. IPDs can be designed as flip chip mountable or wire bondable components and the substrates for IPDs usually are thin film substrates like silicon, alumina or glass. Every passive components are separation and have enough space between each other to reduce the heating effects.

## Effects of vibrations

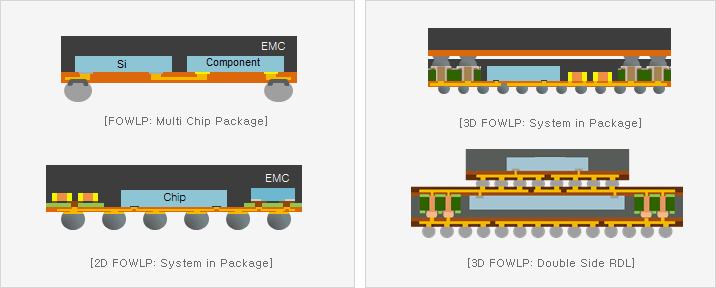
All passive components are soldered separately on the pads, so they reduce the vibrate effects.

## Package size vs I/Os

In my opinion, the package size is depend on the quality of passive components. It can reduce the I/O lead. The same I/O function of different component can be combine to one lead. The less I/O means it can be easy connect with the PCB and easy to fix.

IPD package have advantages in thermal implement and package I/Os.

# SIP – System in Package(系统封装)

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## Thermal implications

Systems-in-package are like [systems-on-chip](https://en.wikipedia.org/wiki/System_on_a_chip" \o "System on a chip) (SoC) but less tightly integrated and not on a single [semiconductor die](https://en.wikipedia.org/wiki/Die_(integrated_circuit)" \o "Die (integrated circuit)). So it pulls down the distance between devices without reducing the functionality to better reduce the thermal impact.

## Package size vs I/Os and Effects of vibrations

SIP is a number of integrated circuits enclosed in a single chip carrier package. Dies containing integrated circuits may be stacked vertically on a substrate. They are internally connected by fine wires that are bonded to the package. Alternatively, with a flip chip technology, solder bumps are used to join stacked chips together. The volume is reduced, the protection property of the chip is improved, and the number of leads is reduced.